CLAIMS:

1. An electronic circuit arrangement comprising a clock fail circuit arranged for receiving a clock signal and generating an error signal upon the absence of the clock signal, characterized in that the electronic circuit arrangement further comprises an asynchronous processor arranged for receiving said error signal and to bring the electronic circuit arrangement in a pre-defined state upon detection of the error signal.

2. An electronic circuit arrangement as claimed in claim 1, characterized in that the asynchronous processor comprises an interrupt input for receiving the error signal and is further arranged to execute software instructions upon reception of the error signal.

3. An integrated circuit comprising an electronic circuit arrangement as claimed in claim 1.

4. A bus station for use in a bus system comprising an electronic circuit arrangement as claimed in claim 1.

5. A bus station as claimed in claim 3, characterized in that the bus station is a bus station for use in a LIN bus system.

6. A method for bringing an electronic circuit arrangement in a predetermined state, whereby the electronic circuit arrangement comprises a clock fail circuit that detects the absence of a clock signal and generates an error signal in response, characterized in that the electronic circuit arrangement further comprises an asynchronous processor that brings the electronic circuit arrangement in the predetermined state.